

INFORMATION DISCLOSURE CITATION PTO-1449				Complete If Known	
				Application Number	10/742,327
				Filing Date	December 18, 2003
				First Named Inventor	Tsern et al.
				Art Unit	3694
				Examiner Name	Cheung, Mary Da Zhi Wang
Sheet	1	of	1	Attorney Docket Number	60809-0146-US

U.S. PATENT DOCUMENTS							
Examiner Initials	Cite No.	Document Number Number - Kind Code ¹	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Filing Date if Appropriate

FOREIGN PATENT DOCUMENTS								
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OTHER NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		BURSKY, "Memory-CPU Interface Speeds Up Data Transfers," Electronic Design, pp. 137-142, March 19, 1992.
		CHOI, "16Mbit Synchronous DRAM with 125Mbyte/sec Data Rate," Symposium on VLSI Circuits, Digest of Technical Papers, pp. 65-66, 1993.
		GARY et al., "The PowerPC™ 603 Microprocessor: A Low-Power Design for Portable Applications," IEEE Design & Test of Computers, Winter, 1994.
		LEE et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," J. of Solid State Circuits, Vol. 29, No. 12, pp. 1491-1496, December 1994.
		LINES et al., "High Speed Circuit Techniques in a 150Hz 64M SDRAM," Proceedings of Memory Technology, Design & Testing Int'l Workshop, San Jose, California, August 11, 1997, pp. 8-11.
		SAEKI et al., "A 2.5ns Clock Access, 250MHz 256Mb SDRAM with Synchronous Mirror Delay," IEEE ISSCC Digest of Technical Papers, pp. 374-375, 476, 1996.

Examiner Signature		Date Considered	
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